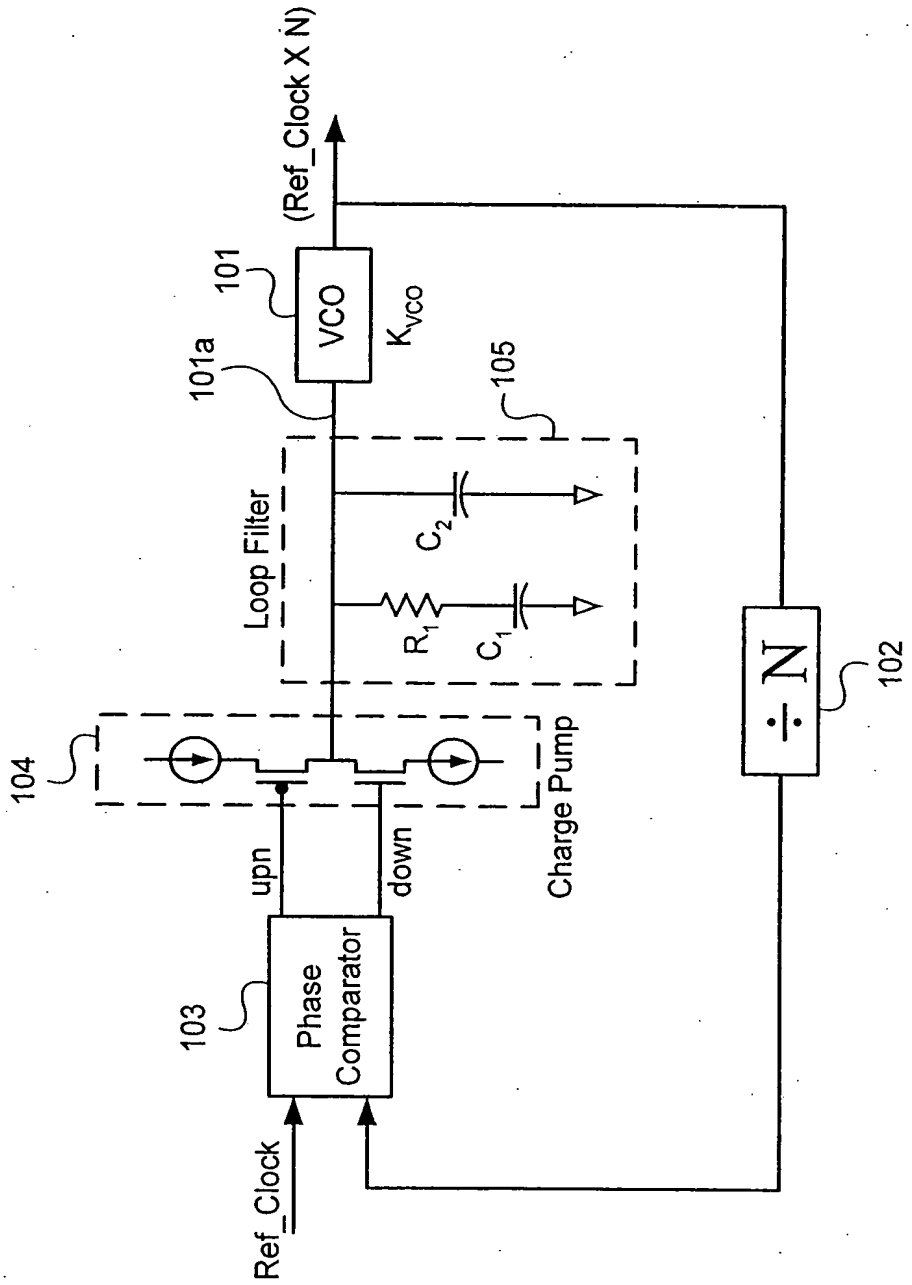

Prior Art
FIG. 1

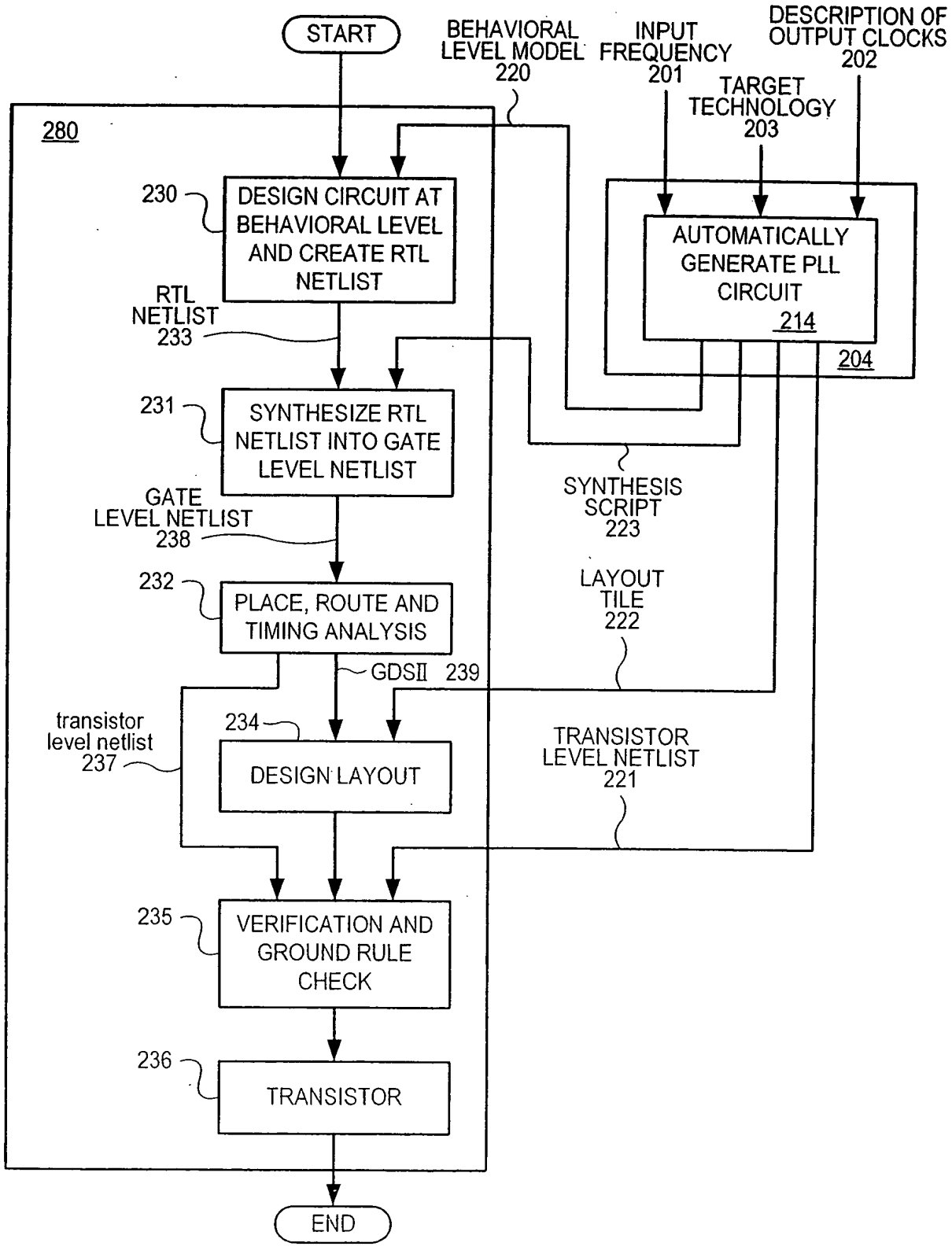
START
BEHAVIORAL LEVEL MODEL 220
INPUT FREQUENCY 201
DESCRIPTION OF OUTPUT CLOCKS 202
TARGET TECHNOLOGY 203
280
230
DESIGN CIRCUIT AT BEHAVIORAL LEVEL AND CREATE RTL NETLIST
AUTOMATICALLY GENERATE PLL CIRCUIT 214
204
RTL NETLIST 233
231
SYNTHESIZE RTL NETLIST INTO GATE LEVEL NETLIST
SYNTHESIS SCRIPT 223
GATE LEVEL NETLIST 238
232
PLACE, ROUTE AND TIMING ANALYSIS
LAYOUT TILE 222
GDSII 239
transistor level netlist 237
234
DESIGN LAYOUT
TRANSISTOR LEVEL NETLIST 221
235
VERIFICATION AND GROUND RULE CHECK
236
TRANSISTOR
END

FIG. 2

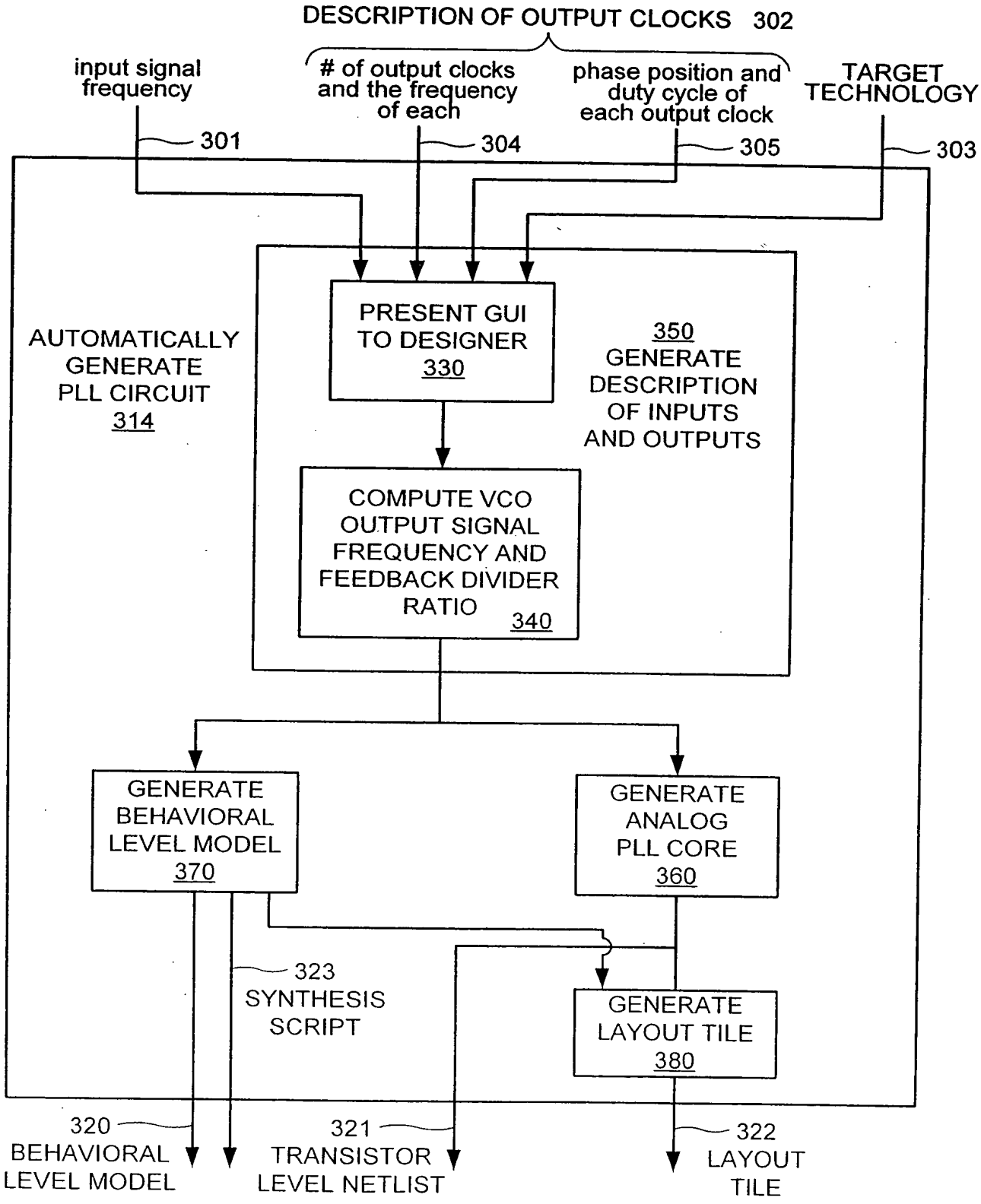
DESCRIPTION OF OUTPUT CLOCKS 302
input signal frequency
301
# of output clocks and the frequency of each
304
phase position and duty cycle of each output clock
305
TARGET TECHNOLOGY
303
AUTOMATICALLY GENERATE PLL CIRCUIT 314
PRESENT GUI TO DESIGNER 330
350 GENERATE DESCRIPTION OF INPUTS AND OUTPUTS
COMPUTE VCO OUTPUT SIGNAL FREQUENCY AND FEEDBACK DIVIDER RATIO 340
GENERATE BEHAVIORAL LEVEL MODEL 370
GENERATE ANALOG PLL CORE 360
323 SYNTHESIS SCRIPT
GENERATE LAYOUT TILE 380
320 BEHAVIORAL LEVEL MODEL
321 TRANSISTOR LEVEL NETLIST
322 LAYOUT TILE

FIG. 3

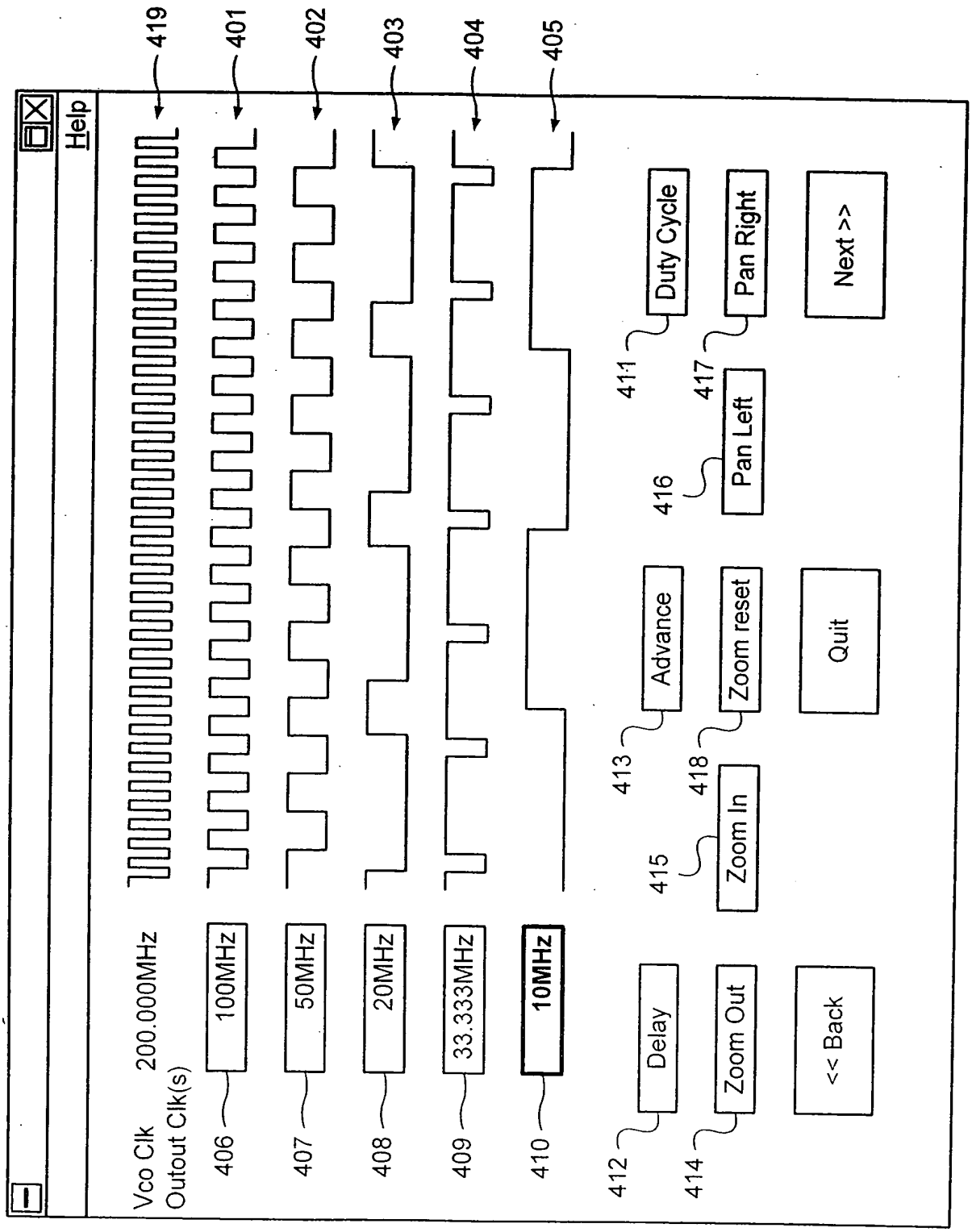
400
Help
Vco Clk 200.000MHz
Outout Clk(s)
419
401
402
403
404
405
406
407
408
409
410
100MHz
50MHz
20MHz
33.333MHz
10MHz
411
Duty Cycle
416
Pan Left
417
Pan Right
412
Delay
413
Advance
414
Zoom Out
415
Zoom In
418
Zoom reset
<< Back
Quit
Next >>

FIG. 4

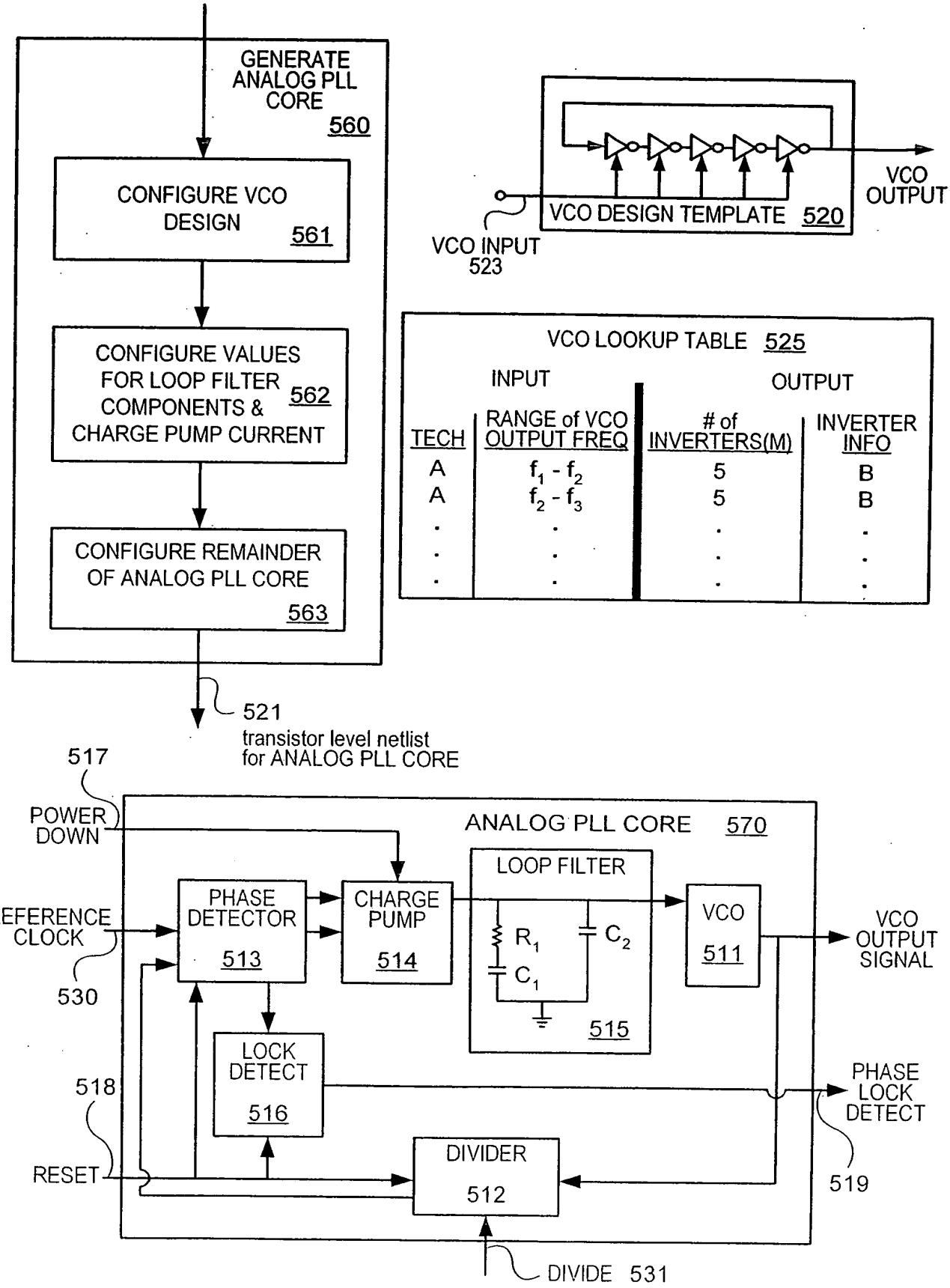
GENERATE ANALOG PLL CORE 560
CONFIGURE VCO DESIGN 561
CONFIGURE VALUES FOR LOOP FILTER COMPONENTS & CHARGE PUMP CURRENT 562
CONFIGURE REMAINDER OF ANALOG PLL CORE 563
521
transistor level netlist for ANALOG PLL CORE
VCO DESIGN TEMPLATE 520
VCO INPUT 523
VCO OUTPUT
VCO LOOKUP TABLE 525
INPUT
OUTPUT
TECH
RANGE of VCO OUTPUT FREQ
# of INVERTERS(M)
INVERTER INFO
A
$f_1 - f_2$
5
B
A
$f_2 - f_3$
5
B
517
POWER DOWN
ANALOG PLL CORE 570
LOOP FILTER
PHASE DETECTOR 513
CHARGE PUMP 514
VCO 511
VCO OUTPUT SIGNAL
REFERENCE CLOCK
530
R_1
C_2
C_1
515
LOCK DETECT 516
518
PHASE LOCK DETECT
519
RESET
DIVIDER 512
DIVIDE 531

FIG. 5

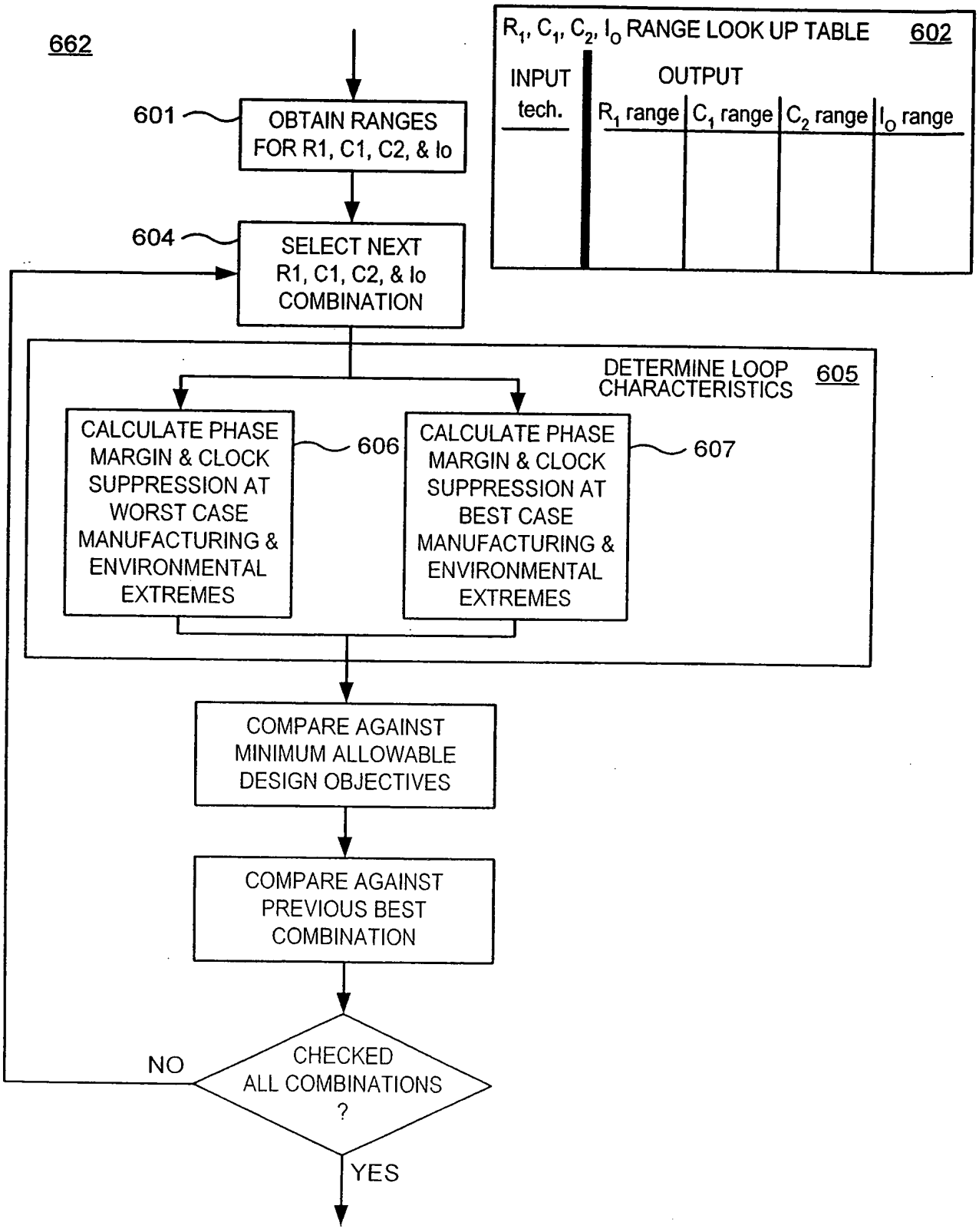
662
601
OBTAIN RANGES FOR R1, C1, C2, & Io
604
SELECT NEXT R1, C1, C2, & Io COMBINATION
R_1, C_1, C_2, I_O RANGE LOOK UP TABLE
602
INPUT tech.
OUTPUT
R_1 range
C_1 range
C_2 range
I_O range
DETERMINE LOOP CHARACTERISTICS
605
CALCULATE PHASE MARGIN & CLOCK SUPPRESSION AT WORST CASE MANUFACTURING & ENVIRONMENTAL EXTREMES
606
CALCULATE PHASE MARGIN & CLOCK SUPPRESSION AT BEST CASE MANUFACTURING & ENVIRONMENTAL EXTREMES
607
COMPARE AGAINST MINIMUM ALLOWABLE DESIGN OBJECTIVES
COMPARE AGAINST PREVIOUS BEST COMBINATION
CHECKED ALL COMBINATIONS ?
NO
YES

FIG. 6

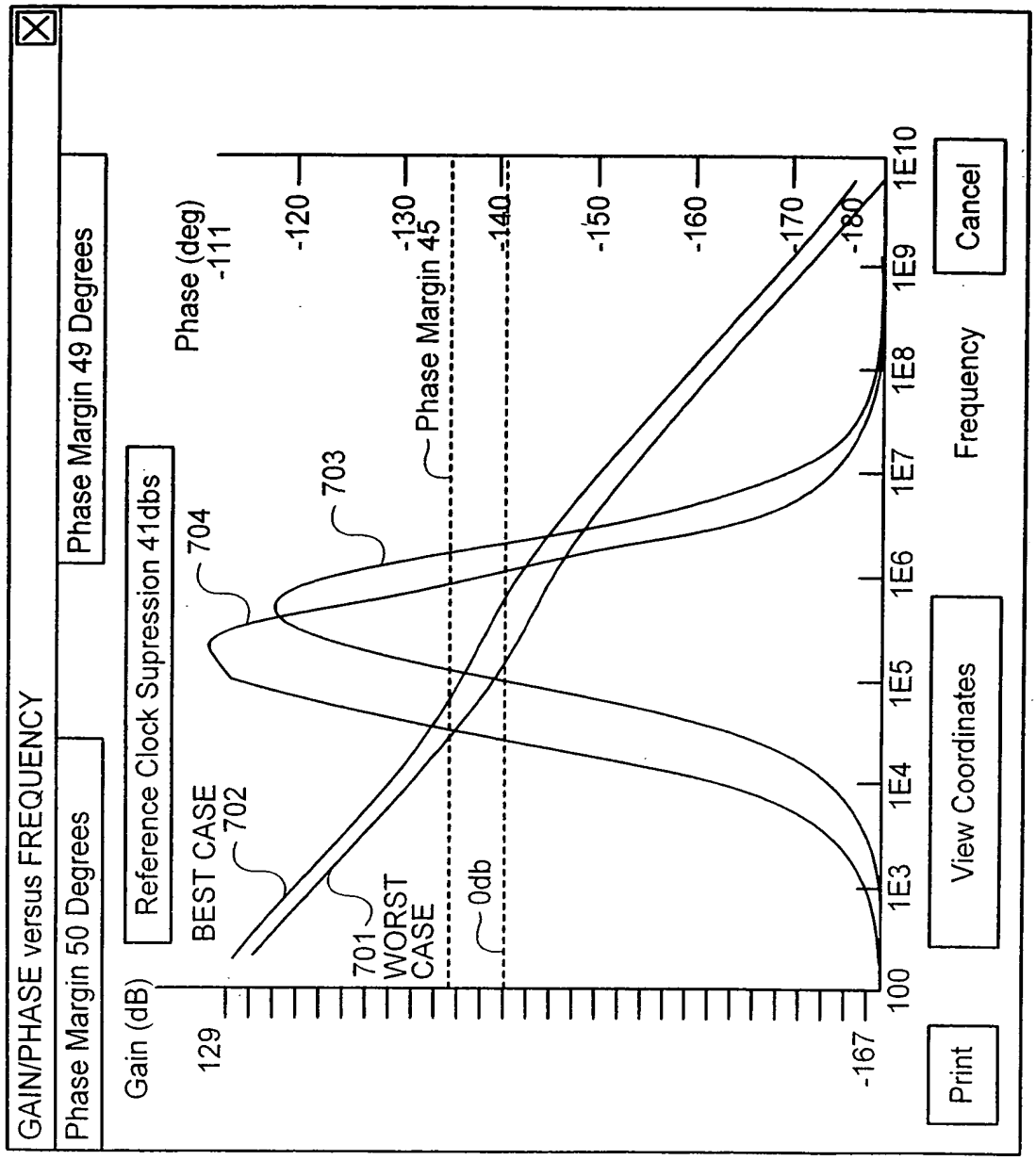
GAIN/PHASE versus FREQUENCY
Phase Margin 50 Degrees
Phase Margin 49 Degrees
Reference Clock Supression 41dbs
Gain (dB)
129
-167
Phase (deg)
-111
-120
-130
-140
-150
-160
-170
-180
Phase Margin 45
0db
BEST CASE
702
WORST CASE
701
703
704
100
1E3
1E4
1E5
1E6
1E7
1E8
1E9
1E10
Frequency
Print
View Coordinates
Cancel

FIG. 7

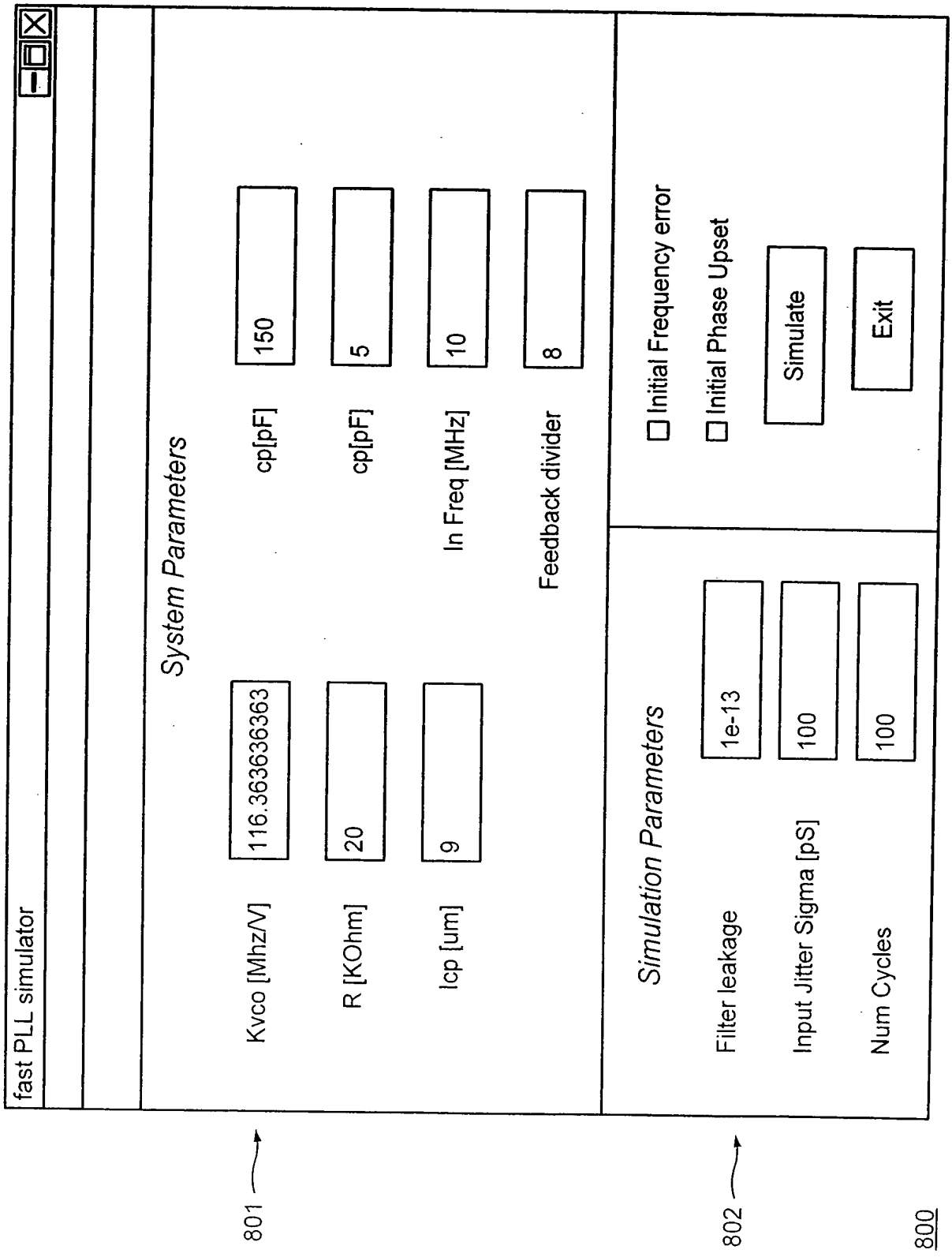
fast PLL simulator
System Parameters
Kvco [Mhz/V]
116.363636363
R [KOhm]
20
Icp [um]
9
cp[pF]
150
cp[pF]
5
In Freq [MHz]
10
Feedback divider
8
Initial Frequency error
Initial Phase Upset
Simulate
Exit
Simulation Parameters
Filter leakage
1e-13
Input Jitter Sigma [pS]
100
Num Cycles
100
801
802
800

FIG. 8

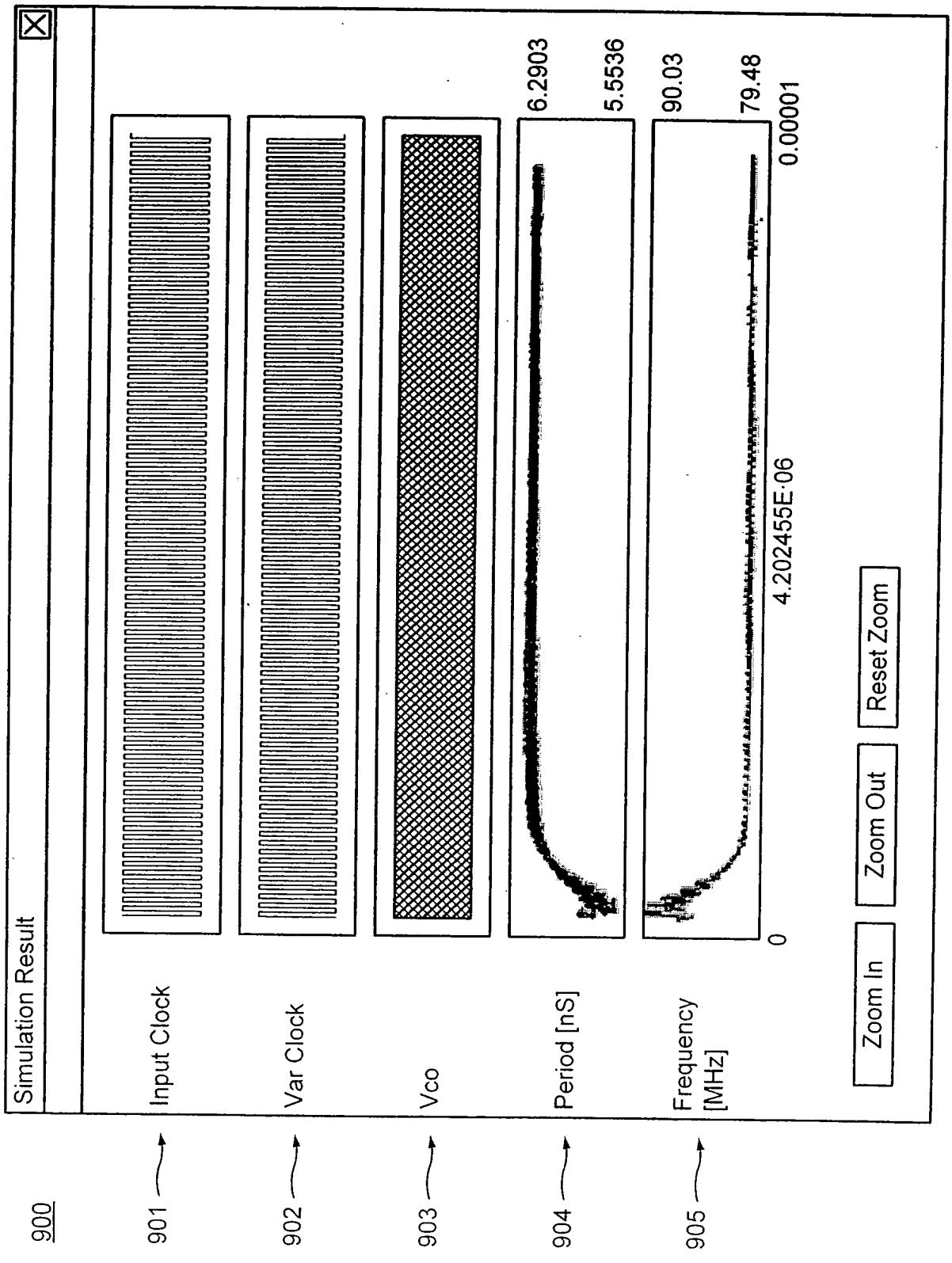
900
901
902
903
904
905
Simulation Result
Input Clock
Var Clock
Vco
Period [nS]
Frequency [MHz]
6.2903
5.5536
90.03
79.48
0.00001
0
4.202455E-06
Zoom In
Zoom Out
Reset Zoom

FIG. 9

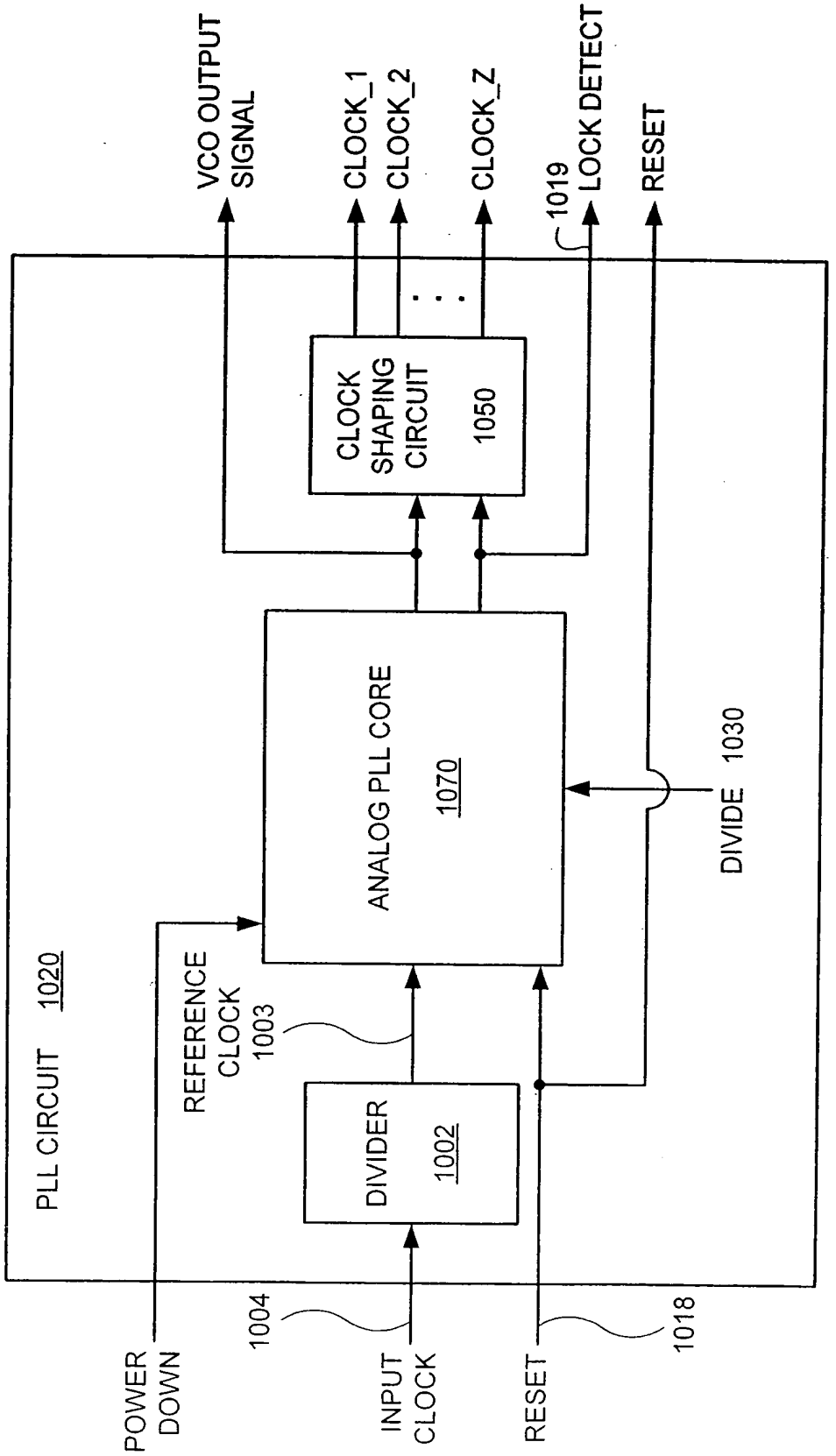
VCO OUTPUT SIGNAL
CLOCK_1
CLOCK_2
CLOCK_Z
1019
LOCK DETECT
RESET
CLOCK SHAPING CIRCUIT 1050
ANALOG PLL CORE 1070
DIVIDE 1030
PLL CIRCUIT 1020
REFERENCE CLOCK 1003
DIVIDER 1002
1004
POWER DOWN
INPUT CLOCK
RESET
1018

FIG. 10

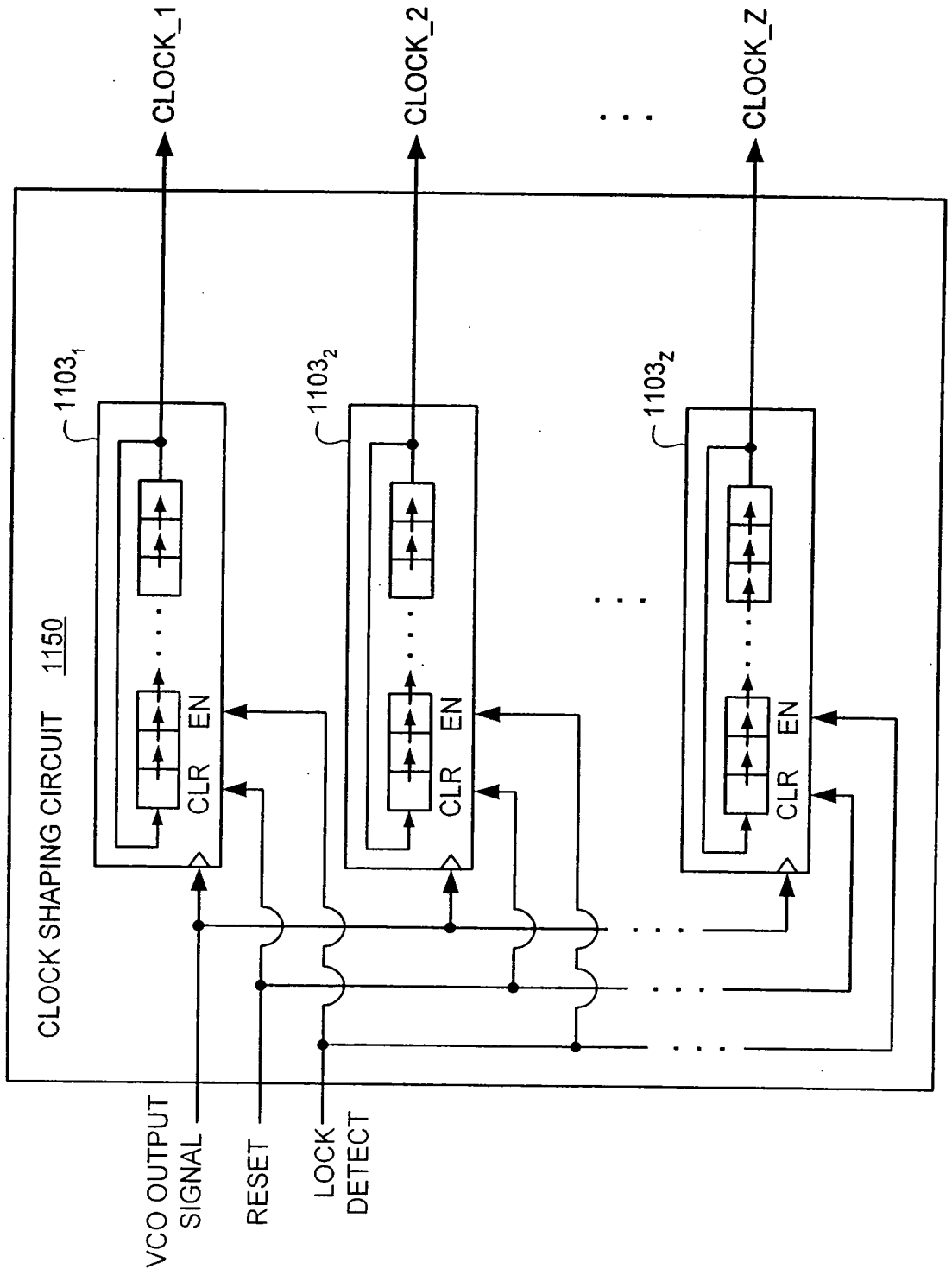
CLOCK_1
CLOCK_2
CLOCK_Z
1103_1
1103_2
1103_Z
CLOCK SHAPING CIRCUIT 1150
CLR EN
CLR EN
CLR EN
VCO OUTPUT SIGNAL
RESET
LOCK DETECT

FIG. 11

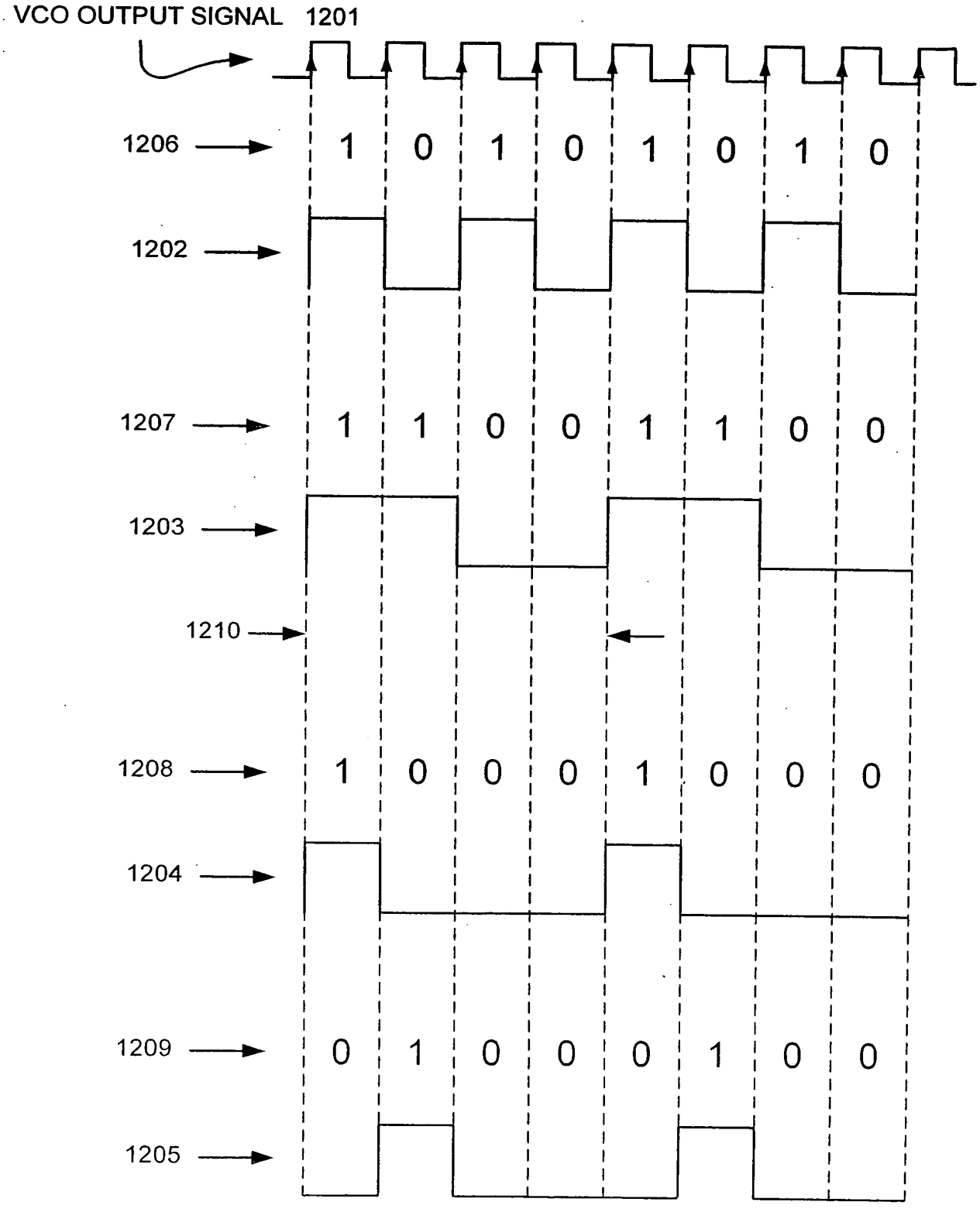
VCO OUTPUT SIGNAL 1201
1206
1 0 1 0 1 0 1 0
1202
1207
1 1 0 0 1 1 0 0
1203
1210
1208
1 0 0 0 1 0 0 0
1204
1209
0 1 0 0 0 1 0 0
1205

FIG. 12

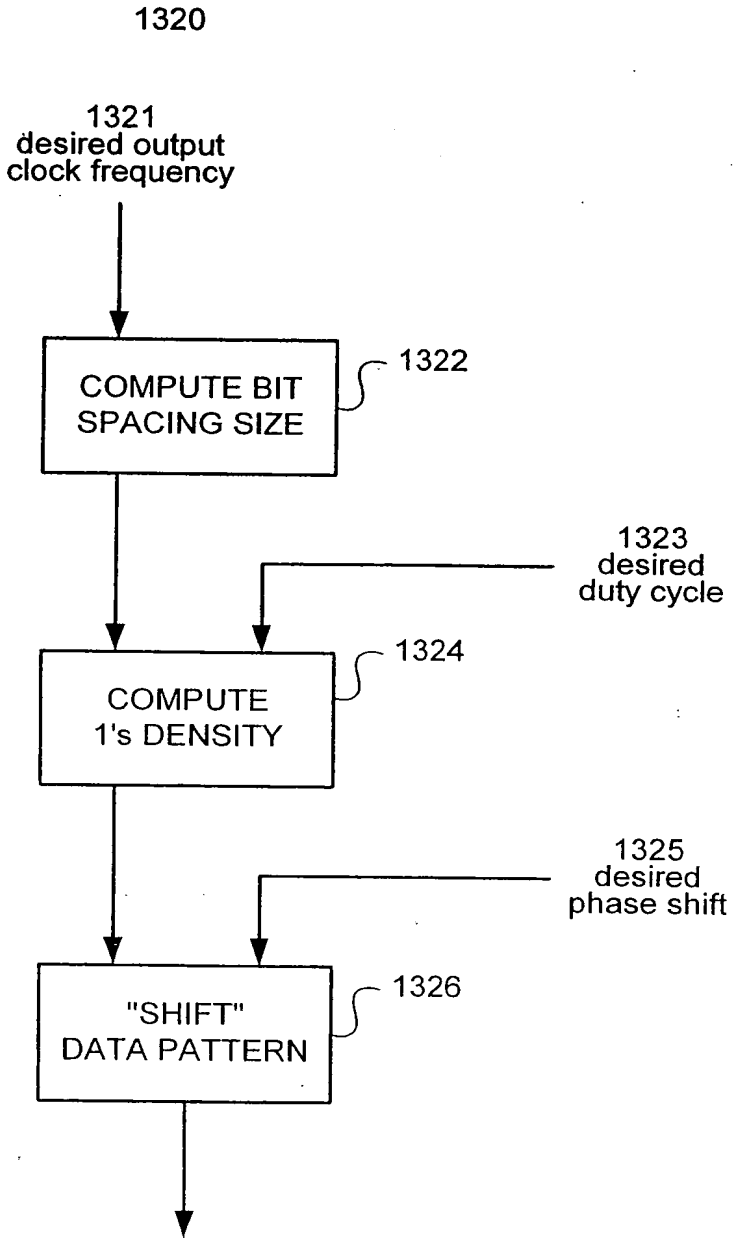
1320
1321
desired output
clock frequency
COMPUTE BIT
SPACING SIZE
1322
1323
desired
duty cycle
COMPUTE
1's DENSITY
1324
1325
desired
phase shift
"SHIFT"
DATA PATTERN
1326

FIG. 13

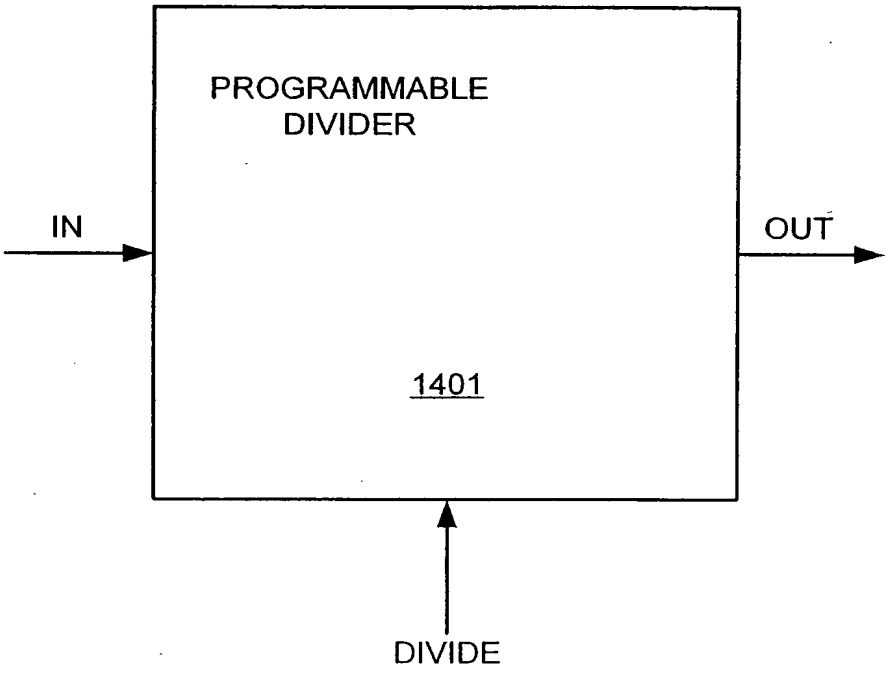

FIG. 14

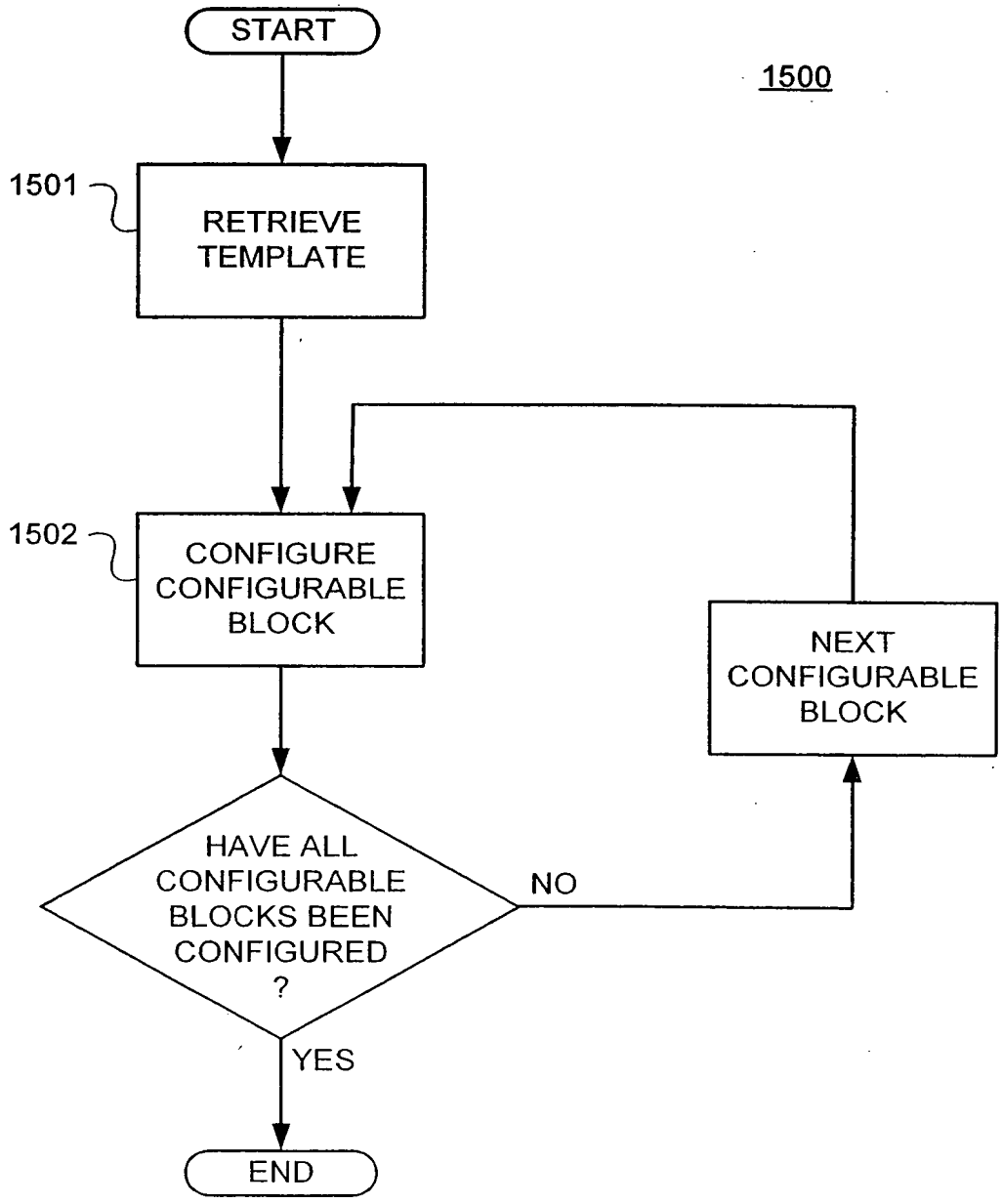
START
1500
1501
RETRIEVE TEMPLATE
1502
CONFIGURE CONFIGURABLE BLOCK
NEXT CONFIGURABLE BLOCK
HAVE ALL CONFIGURABLE BLOCKS BEEN CONFIGURED ?
NO
YES
END

FIG. 15

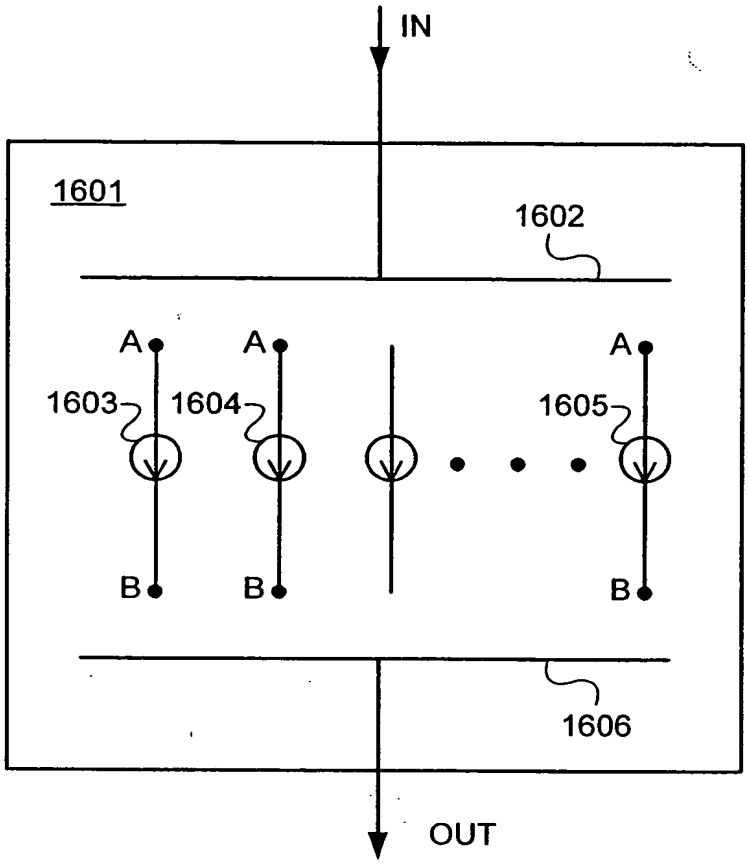

FIG. 16A

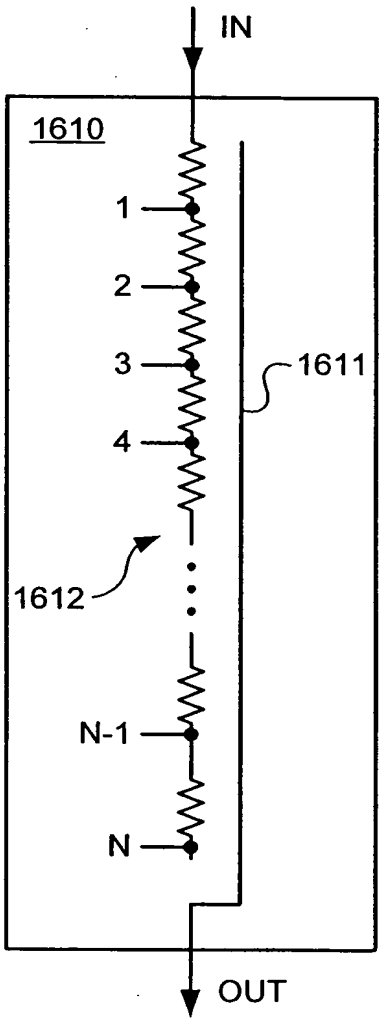

FIG. 16B